TEXAS INSTRUMENTS

Designing With the TL5001 PWM Controller

Application Report

1995

Mixed-Signal Products

SLVA034A

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ABSTRACT

Electrical and electronic products today are required to be lighter and smaller, use less power, and cost less. Because of these requirements, manufacturers are turning more and more to small high-frequency dc-to-dc converters for power-supply solutions. The TL5001 is a pulse-width-modulation (PWM) control integrated circuit, which with a few external components can be used to implement such converters that can operate at frequencies up to 400 kHz.

INTRODUCTION

The TL5001 integrated circuit incorporates all the PWM-control functions in a compact 8-pin package, including:

- Oscillator/triangle-wave generator
- PWM comparator with adjustable dead-time control input
- Open-collector output-drive transistor
- 1-V temperature-stable reference
- Wide-bandwidth error amplifier
- Short-circuit protection (SCP)
- Undervoltage lockout (UVLO)

In addition, the TL5001 operates over a 40-kHz to 400-kHz frequency range with supply voltages ranging from 3.6 V to 40 V and typically consumes only 1 mA of supply current.

This application report demonstrates the design of three simple step-down (buck) converters. The designs include: two converters operating from 12 V and delivering 5 V at 3 A, 3.3 V at 3 A, and one that operates from 5 V and delivers 3.3 V at 0.75 A, using the TL5001 and a few external components.

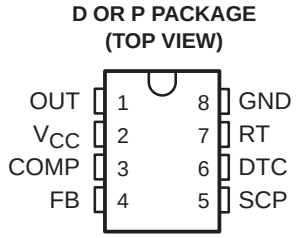
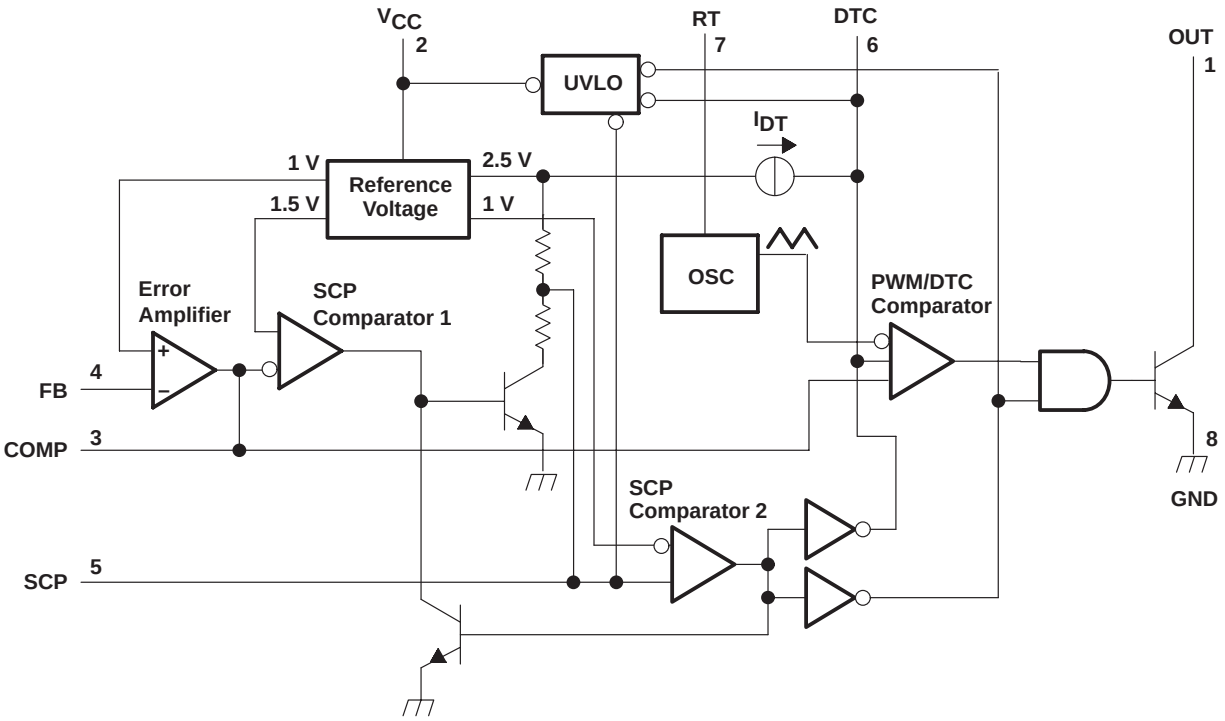


Figure 1. Package Layout



SCP = Short-circuit protection
UVLO = Undervoltage lockout protection

Figure 2. Functional Block Diagram

EXAMPLE 1: 12-V to 5-V at 3-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 8.

Specifications

Input voltage range, V_I	10 V to 15 V
Output voltage, V_O	5 V
Output current, I_O	0 A to 3 A
Output ripple voltage	≤50 mV
Regulation	1%
Efficiency	≥80%
Ambient temperature range, T_A	0°C to 55°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down converter operating at 200 kHz.

Duty-Cycle Estimates

Before starting the detailed design, it is useful to estimate the duty cycle, D (ratio of the power-switch conduction time to the period of the operating frequency), for various input voltages. The duty cycle for a step-down converter operating in continuous mode is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume V_d = 0.6 V)
V_{sat} = power-switch conduction voltage (assume V_{sat} = 0.5 V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for V_I = 10, 12, and 15 V is 0.59, 0.49, and 0.39, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose the inductance value to maintain continuous-mode operation down to 10% of rated output current.

$$\Delta I_O = 2 \times 0.1 \times I_{O(max)} = 2 \times 0.1 \times 3 = 0.6 \text{ A peak-to-peak}$$

The ripple current is simply the product of the inductor voltage and t_{on}, the power-switch conduction time, divided by the inductor value.

$$\Delta I_O = \frac{V_{ind} \times t_{on}}{L1} = \frac{V_{ind}\ DTs}{L1}$$

where Ts = period of the converter operating frequency.

The inductor voltage during t_{on} is the input voltage minus V_{sat}, the power-switch conduction voltage, minus the output voltage. Solving for L1,

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)(D)\ (t)}{\Delta I_O} = \frac{(15 - 0.5 - 5)\ (0.39)\ \left(5 \times 10^{-6}\right)}{0.6} = 30.87\ \mu H$$

Because the core is too large, there are not many off-the-shelf surface-mount devices for this design. A 27-μH inductor (27 turns of 22-gauge magnet wire on a Micrometals T50-26B powdered-iron toroid) was selected because it was readily available.

Output-Filter-Inductor Selection

Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficently high.

Capacitor

The output capacitor is selected to limit ripple voltage to the level required by the specification. The three elements of the capacitor that contribute to ripple are: equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance. Normally, in designs of this type, it is necessary to provide a great deal of capacitance to get ESR to acceptable levels. ESL, which can be a problem at high frequencies, can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

Assuming all the inductor ripple current flows through the filter capacitor and the ESR is zero, the capacitance needed to limit the ripple to 50 mV peak-to-peak is:

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.6}{(8)\left(200 \times 10^3\right)(0.05)} = 7.5\ \mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.6} = 83\ m\Omega$$

Capacitor ripple current is seldom a problem in low-voltage converters unless a large number of devices are paralleled. However, to be on the safe side, the rms current is established as:

$$\Delta I_{O(rms)} = 0.6 \times 0.289 = 0.17\ \text{Arms}$$

The output-filter capacitor(s) should be rated for: at least ten times the calculated minimum capacitance, an ESR 30% to 50% lower than the calculated maximum, a 0.5-Arms-or-greater ripple-current rating at 100 kHz and 85°C, and a 7.5-V or greater voltage rating.

Use one 220-µF 10-V OS-CON SA-series device, even though it is in a lead-mounted radial package. The ESR is 35 mΩ (at 100 kHz) and the 85°C ripple-current rating is 2.36 Arms. Where package height and/or surface-mount packaging is critical, two solid tantalum-chip 100-µF 10-V devices with 100-mΩ ESR and 1.1-Arms ripple-current rating from either the AVX TPS series or the Sprague 593D series connected in parallel work well.

Output-Filter-Capacitor Selection

Three capacitor technologies: low-impedance aluminum, organic semiconductor, and solid tantalum, are suitable for low-cost commercial applications such as this one. Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but ESR is higher than the other two and there are currently no surface-mount devices suitable for this application. Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds – a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

Power-Switch Design

The power-switch design includes: selecting the power switch, catch rectifier, and rectifier-snubbing network (if needed), calculating power dissipations and junction temperatures, and ensuring the semiconductors have proper heat sinking.

Power Switch

The design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. Based on the preliminary estimate, $r_{DS(on)}$ should be less than 0.5 V ÷ 3 A = 167 mΩ with a 10-V gate drive and the drain-to-source breakdown voltage appropriate for a 15-V supply. Surface-mount packaging is also desirable.

The IRF9Z34S is a 60-V p-channel MOSFET in a power surface-mount package with $r_{DS(on)}$ = 140 mΩ maximum with a 10-V gate drive.

Power dissipation, which includes both conduction and switching losses, is given by:

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

Where t_{r+f} = total MOSFET switching time (turn-on and turnoff) and $r_{DS(on)}$ is adjusted for temperature.

Assuming the drive circuit is adequate for t_{r+f} = 100 ns and the junction temperature is 125°C with a 55°C ambient, the $r_{DS(on)}$ adjustment factor is 1.6.

$$P_D = \left(3^2\right)(0.14 \times 1.6)(0.59) + (0.5)(10)(3)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)$$

$$P_D = 1.19 + 0.30 = 1.49 \text{ W}$$

Conduction losses are dominant in this application but may not be in others. It is good practice to check dissipation at the extreme limits of input voltage to find the worst case.

The thermal impedance $R_{\theta JA}$ = 40°C/W for FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (40 \times 1.49) = 115°C$$

Bipolar Versus MOSFET Power Transistors

Each of the three designs presented in this report could be implemented with bipolar or MOSFET transistors as the power switch. Bipolars are inexpensive and can perform well in low-voltage applications such as these, but designing a drive circuit to realize the performance is not a trivial effort. Furthermore, complex base-drive schemes can eliminate much, if not all, of the cost advantage. MOSFETs were selected for this application because the fast switching times required for high-frequency operation are acheived with relatively simple, low-component-count gate drive circuits, and the focus in this report is the controller design.

Catch Rectifier

The catch rectifier conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low-forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low-voltage outputs is usually a Schottky rectifier.

The breakdown voltage must be 20 V or greater to handle the 15-V input; the current rating must be at least 3 A (normally the current rating will be much higher than the output current because the power limits the number of acceptable devices); and a surface-mount package is extremely desirable.

The 50WQ03F is a 5.5-A, 30-V Schottky in a DPAK, power surface-mount package. Care must be taken to ensure that the rectifier maximum junction temperature is not exceeded. The first step in determining the rectifier junction temperature is to estimate worst-case power dissipation. Neglecting leakage current and assuming the ripple current in the inductor is much less than the output current, the catch-rectifier power dissipation is:

$$P_D = I_O \times V_d \times (1 - D)$$

where V_d is the rectifier conduction drop. Worst-case dissipation occurs at high line where D is minimum. The 50WQ03F has a maximum forward drop of 0.55 V at a forward current of 3 A and a junction temperature of 125°C.

$$P_D = 3 \times 0.55 \times (1 - 0.39) = 1 \text{ W}$$

The thermal impedance $R_{\theta JA}$ = 50°C/W when mounted on FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (50 \times 1) = 105°C$$

Catch-Rectifier Snubber Network

Step-down converters almost universally suffer from ringing on the voltage waveform at the node where the power-switch drain, output inductor, and catch-rectifier cathode connect. The ringing, which results from driving parasitic inductances and capacitances with fast rise-time waveforms, ranges in severity from objectionable to unacceptable depending on component selection and PCB layout. An RC-snubber damping network in parallel with the catch rectifier is by far the simplest way to minimize or eliminate the problem. Since deleting components from a printed-circuit layout is usually easier than adding them, the safest strategy is to include the network in the initial design and delete the components if they prove unnecessary.

The initial design is straightforward, but the PCB layout may necessitate component-value adjustments during the prototype phase. The capacitor value chosen is 4 to 10 times greater than the rectifier junction capacitance; higher values improve the snubbing but dissipate more power. The 50WQ03F has a typical junction capacitance of 180 pF, and a snubber-capacitor value should be between 750 pF and 1.8 nF. Use C8 = 1.2 nF for convenience. Rectifiers normally ring in the range from 1 to 50 MHz. Choose the snubber resistor, R10, for a 50-ns time constant:

$$R10 = \frac{50 \times 10^{-9}}{C8} = \frac{50 \times 10^{-9}}{1.2 \times 10^{-9}} = 41.7\ \Omega \Rightarrow \text{Use } 43\ \Omega$$

Because the capacitor is charged and discharged each cycle, the power dissipation in R10 is:

$$(2)(C8)\left(V_I^2\right)\left(\frac{f_s}{2}\right) = (2)\left(1.2 \times 10^{-9}\right)\left(15^2\right)\left(\frac{200 \times 10^3}{2}\right) = 54 \text{ mW}$$

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, the dead-time control voltage, the soft-start timing, and the short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

Resistance value R1 is selected to set the oscillation frequency to 200 kHz. Select R1 = 43 kΩ from the graph shown in Figure 3.

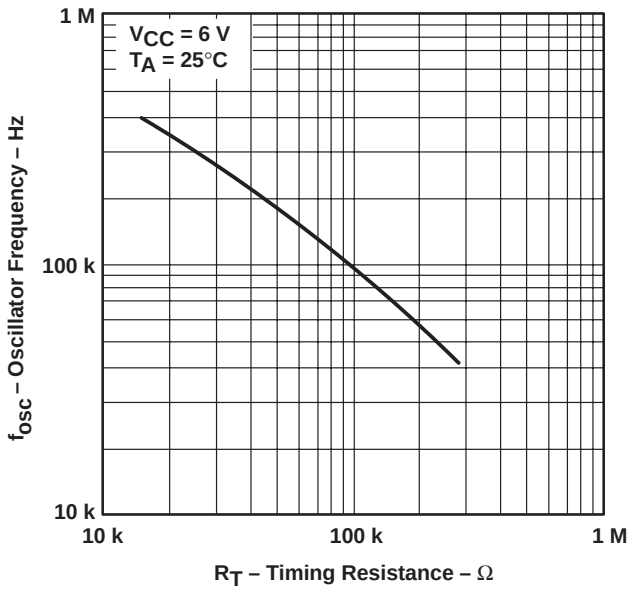


Figure 3. Oscillator Frequency Versus Timing Resistance

Dead-Time Control

Dead-time control provides a minimum period of time during each cycle when the power switch cannot be on; i.e., it limits the duty cycle to some value less than 100%. Even though dead time is not necessary in this application, a small amount is provided to minimize the surge current that would result from a short circuit while the protection circuit is timing out.

The dead time is set by connecting a resistor, R2, between DTC and GND. A constant current I_{DT} flows out of DTC generating a voltage, V_{DT}. I_{DT} is controlled by the current I_T that flows out of RT (this current is normally equal to I_T, but varies slightly with frequency and the peak amplitude of V_{DT}). The maximum duty cycle is 0.59. Typically, the actual duty cycle is set slightly higher to allow for parameter tolerances. For this design, a duty cycle of 0.70 is chosen. See Figure 4 to find the maximum and minimum ramp-voltage levels, $V_{O(100\%)}$ and $V_{O(0\%)}$; R2 is calculated from the following expression (R_{DT}, R_t in kΩ, D in decimal):

$$R2 = (R1 + 1.25)\left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right]$$

$$= (43 + 1.25)[0.7(1.4 - 0.6) + 0.6] = 51.3\ k\Omega$$

A value of 51 kΩ is used for R2.

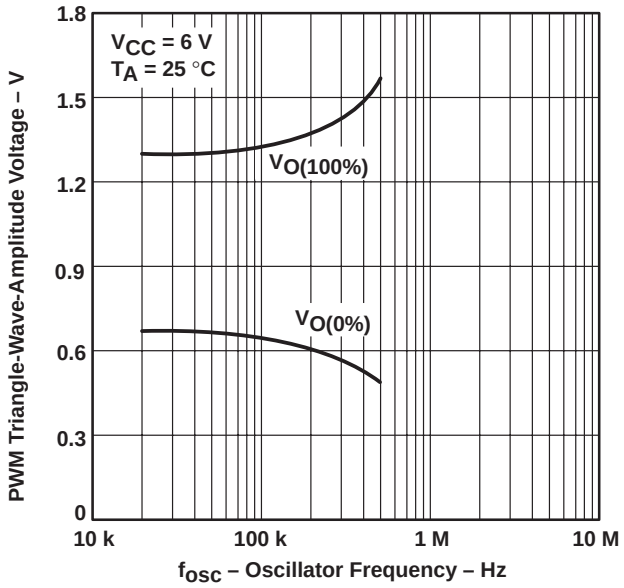


Figure 4. PWM Triangle-Wave-Amplitude Voltage Versus Oscillator Frequency

Soft-Start Timing

Soft start is implemented by adding a capacitor in parallel with the dead-time control resistor, R2. A start-up time of 5 ms is chosen.

$$C5 = \frac{t_r}{R2} = \frac{5 \times 10^{-3}}{51 \times 10^{3}} = 0.1\ \mu F$$

SCP Timing

In normal operation, SCP and the timing capacitor, C4, are clamped to approximately 185 mV. Under short-circuit conditions, C4 is allowed to charge. If the voltage across C4 reaches 1 V, the SCP latch is activated and the converter is shut down. The protection-enable period, t_{pe}, must be longer than the dc/dc converter start-up time, or the converter will never come up. Because the soft start is designed to bring the converter up within 5 ms, t_{pe} = 75 ms should work well. C4 is given by (t_{pe} in s, C4 in μF);

$$C4 = 12.46 \times t_{pe} = 12.46 \times 0.075 = 0.935\ \mu F \Rightarrow 1\ \mu F$$

Output Sense Network

The output sense network is a resistive divider connected between the converter output and ground with the divider output connected to the TL5001 FB terminal (refer to Figure 6). The divider ratio is chosen for a 1-V output (the TL5001 reference voltage) when the converter output is at the desired value.

Establishing the proper divider ratio is critical, but selecting values for the sense network is somewhat arbitrary. Choosing the values too high can result in converter-output-voltage accuracy problems because the error-amplifier input-bias current loads the network. Values that are too low can dissipate too much power, drain too much power from limited power sources such as batteries, or lead to loop-compensation-capacitor values that are too high to be practical. As a rule, a divider current approximately 1000 times greater than the maximum error-amplifier input current is chosen. Resistors with 1% tolerances and low and/or reasonably well-matched temperature coefficients are recommended to minimize the output voltage tolerance.

Because the worst-case TL5001 input bias current is 0.5 μA, the divider current should be approximately 1000 × 0.5 μA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is V_O – 1 V = 4 V.

$$R6 = \frac{1\ V}{0.5\ mA} = 2\ k\Omega$$

$$R5 = \frac{\left(V_O - 1\ V\right)}{0.5\ mA} = \frac{5 - 1}{0.5 \times 10^{-3}} = 8\ k\Omega$$

Since they are readily available and provide the right divider ratio, R5 = 7.50 kΩ and R6 = 1.87 kΩ are used.

Loop Compensation

The loop-compensation design procedure consists of shaping the error-amplifier frequency response with external components to stabilize the dc/dc converter feedback control loop without destroying the control-loop ability to respond to line and/or load transients. A detailed treatment of dc/dc converter stability analysis and design is well beyond the scope of this report; however, several references on the subject are available. The following is a simplified approach to designing networks to stabilize continuous-mode buck converters that works well when the open-loop gain is below unity at a frequency much lower than the frequency of operation.

Ignoring the error-amplifier frequency response, the response of the pulse-width modulator and power switch operating in continuous mode can be modeled as a simple gain block. The magnitude of the gain is the change in output voltage for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). Typically, increasing the COMP voltage from 0.6 V to 1.4 V increases the duty cycle from 0 to 100% and the output voltage from 0 V to approximately 12 V at the nominal input voltage. The gain, A_{PWM}, is:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{(12 - 0)}{(1.4 - 0.6)} = 15 \Rightarrow 24 \text{ dB at nominal input}$$

Similarly, the gain is 22 dB at low line and 25 dB at high line. Converters with wider input ranges, 2:1 or more, need to check for stability at several line voltages to ensure that gain variation does not cause a problem.

The output filter is an LC filter and functions accordingly. The inductor and capacitor produce an underdamped complex-pole pair at the filter resonant frequency and the capacitor ESR (R_S) puts a zero in the response above the resonant frequency. The complex poles are located at:

$$\frac{1}{2\ \pi\ \sqrt{LC}} = \frac{1}{2\ \pi\ \sqrt{\left(27 \times 10^{-6}\right)\left(220 \times 10^{-6}\right)}} = 2.06 \text{ kHz}$$

The zero is located at:

$$\frac{1}{2\ \pi\ R_S C} = \frac{1}{(2\ \pi)(0.035)\left(220 \times 10^{-6}\right)} = 20.7 \text{ kHz.}$$

Figure 5 includes gain and phase plots of the open-loop response (error amplifier not included) obtained from a simple SPICE simulation.

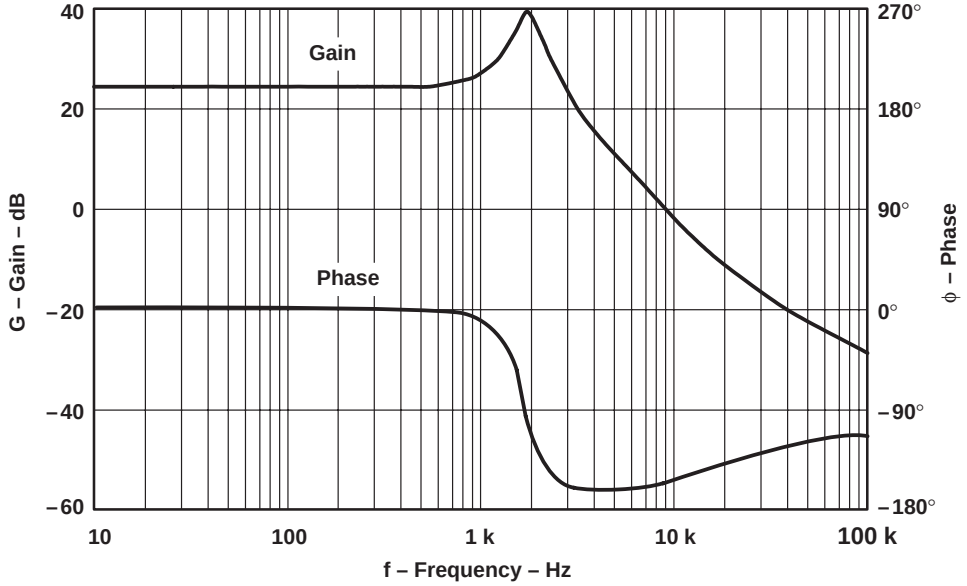


Figure 5. Uncompensated Open-Loop Response

The presence of the complex-pole pair is evident from the resonant peaking in the gain at 2 kHz and the rapid phase transition in the vicinity of 2 kHz. The zero is hard to see in the gain plot but shows up well in the phase response; the complex poles provide –180° of phase shift at 20 kHz and the zero adds 45° for a net of –135°.

Unless the designer is trying to meet an unusual requirement, such as very wide band response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage; compensation zeros are added near the filter poles to correct for the sharp change in phase encountered near the filter-resonant frequency; and an open-loop unity-gain frequency is selected well beyond the filter-resonant frequency but 10% or less than the converter operating frequency. In this instance, a unity-gain frequency (f_T) of approximately 20 kHz is chosen to provide good transient response. Figure 6 shows a standard compensation network chosen for this example.

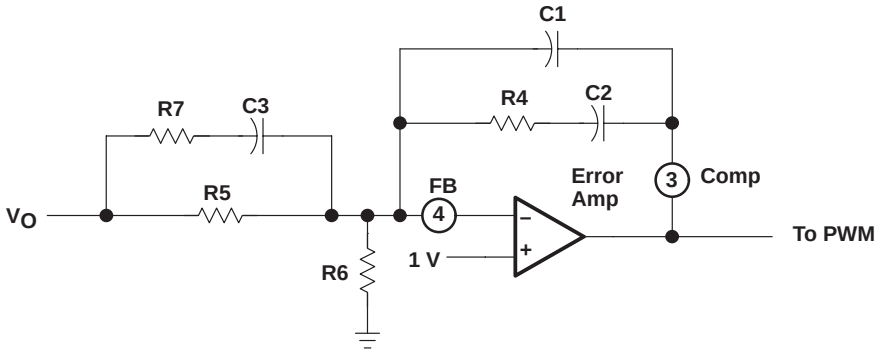


Figure 6. Compensation Network

Assuming an ideal amplifier, the transfer function is:

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C2 + C1)}\right]\left[\frac{[S(R5 + R7)\ C3 + 1]\ (S\ R4\ C2 + 1)}{(S\ R7\ C3 + 1)\left[S\ R4\ \left(C1 \parallel C2\right) + 1\right]}\right]$$

The integrator gain, $1/[R5 \cdot (C2 + C1)]$, establishes the open-loop unity-gain frequency. The zeros are located at approximately the same frequency as the output-filter poles to compensate for the gain reduction and phase shift. The pole at $1/(2\pi \cdot R7 \cdot C3)$ is positioned at approximately the same frequency as the zero in the output filter to maintain the 20 dB-per-decade roll-off in the gain response. The final pole at $1/(2\ \pi \cdot R4 \cdot C1 \parallel C2)$ is placed at a frequency between half of the operating frequency and the operating frequency to minimize high-frequency noise at the pulse-width-modulator input. The last pole is not always necessary but should be included in the design until the need is established.

The sum of the gains of the modulator, the LC filter, and the error amplifier is 0 dB at the unity-gain frequency. The gain of the modulator/LC filter at 20 kHz may be calculated or obtained from a bode plot using straight-line approximations or from a simple SPICE simulation. As shown in Figure 5, the modulator/filter gain is –12 dB at 20 kHz.

The compensation network has two zeros at 2 kHz to cancel out the LC filter poles. These two zeros contribute a gain of 40 dB at 20 kHz; therefore, the gain contributed by the compensation-network integrator needs to be –28 dB [0 – (–12 +40) = –28]. The integrator gain of –28 dB translates to a voltage gain of 0.0398.

$$\frac{1}{(2\ \pi)\left(f_T\right)(R5)(C2 + C1)} = 0.0398\ \left(\text{at } f_T\ =\ 20\ \text{kHz}\right)$$

In practice, C2 >> C1,

$$C2 = \frac{1}{(2\pi)\left(f_T\right)(R5)(0.0398)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(7.5 \times 10^3\right)(0.0398)} = 0.027\ \mu F$$

R4 is chosen to position a zero at 2 kHz.

$$R4 = \frac{1}{(2\pi)(f)(C2)} = \frac{1}{(6.28)\left(2 \times 10^3\right)\left(0.027 \times 10^{-6}\right)} = 2.95\ k\Omega \Rightarrow \text{Use } 3.0\ k\Omega$$

R7 and C3 are chosen to provide a zero, f_{Z1}, at 2 kHz and a pole, f_{P1}, at 20 kHz.

$$f_{Z1} = \frac{1}{2\pi(R5 + R7)\ C3} = \frac{1}{[(2\pi)(R5)(C3)] + [(2\pi)(R7)(C3)]}$$

$$f_{P1} = \frac{1}{(2\pi)\ (R7)\ (C3)}$$

After algebraic manipulation:

$$(2\pi)(R7)(C3) = \frac{1}{f_P}$$

$$C3 = \frac{\frac{1}{f_Z} - \frac{1}{f_P}}{(2\pi)(R5)} = \frac{\left[\frac{1}{2\times10^3} - \frac{1}{20\times10^3}\right]}{(6.28)\left(7.5 \times 10^3\right)} = 0.0096\ \mu F \Rightarrow \text{Use } C3 = 0.01\ \mu F$$

$$R7 = \frac{1}{(2\pi)\left(f_P\right)(C3)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(0.01 \times 10^{-6}\right)} = 796\ \Omega \Rightarrow \text{Use } 820\ \Omega$$

C1 is chosen to provide the pole, f_{P2}, at 100 kHz. Assuming C3 >> C1.

$$C1 = \frac{1}{(2\pi)\left(f_{P2}\right)(R4)} = \frac{1}{(6.28)\left(100 \times 10^3\right)(3000)} = 531\ pF \Rightarrow \text{Use } 470\ pF$$

Results of the compensated-loop response are shown in Figure 7.

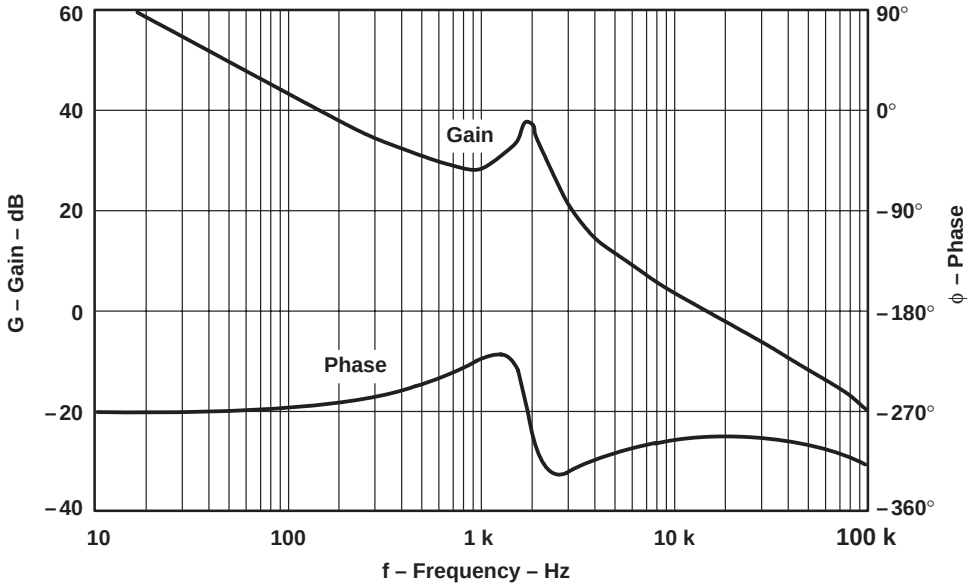
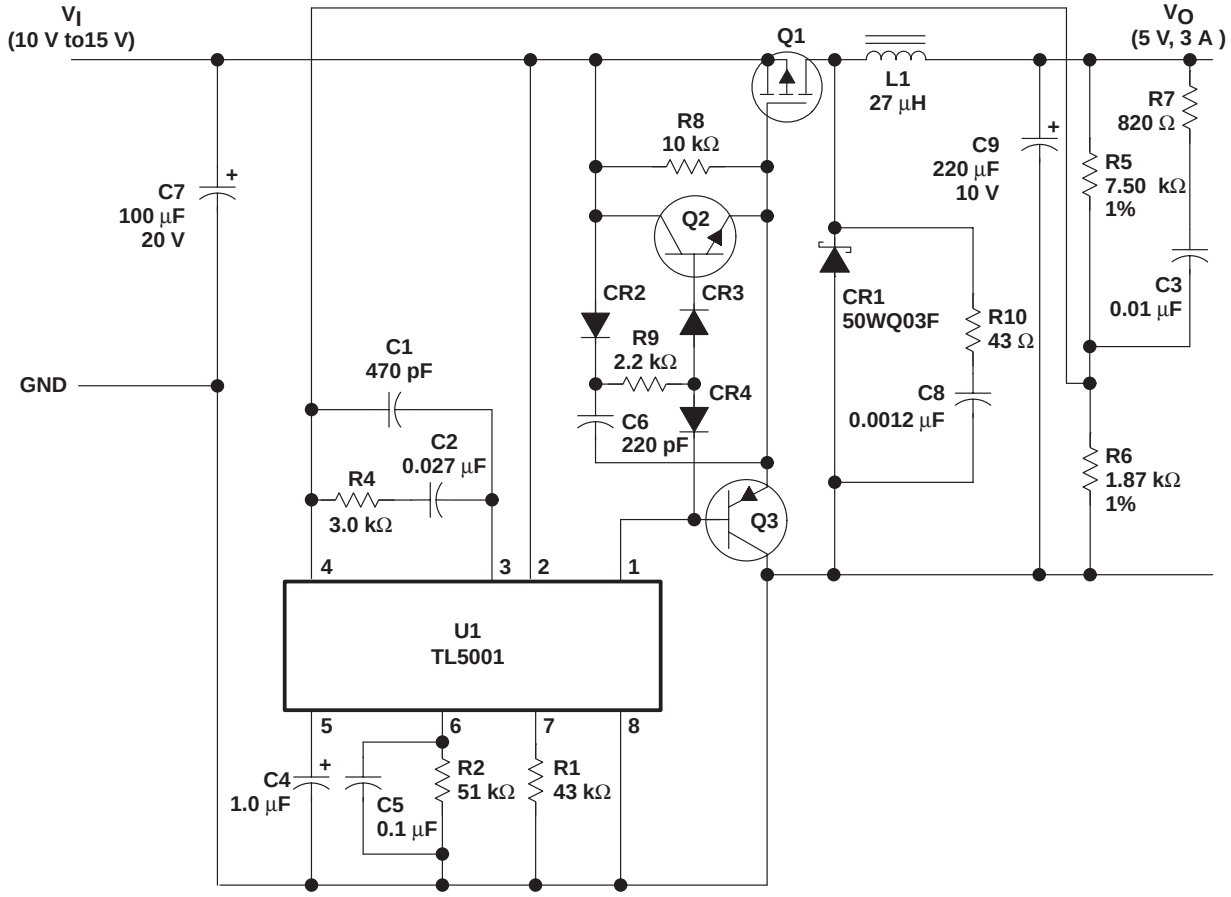


Figure 7. Compensated-Loop Response

Summary

The schematic (Figure 8), bill of materials, and test results for the completed design are provided in this summary.



Q1 – IRF9Z34S
Q2 – PMBT2222APH
Q3 – PMBT2907APH
All diodes are PMBD914PH, unless otherwise specified.
R3 – Not used

Figure 8. 12-V to 5-V at 3-A Converter

Table 1. Example 1: Bill of Materials

REF DES	PART NO.	DESCRIPTION	MFG
U1	TL5001	IC, PWM Controller	Texas Instruments
C1		Capacitor, Ceramic, 470 pF, 50 V, 10%	
C2		Capacitor, Ceramic, 0.027 μF, 50 V, 10%	
C3		Capacitor, Ceramic, 0.01 μF, 50 V, 10%	
C4		Capacitor, Tantalum, 1.0 μF, 20 V, 10%	
C5		Capacitor, Ceramic, 0.10 μF, 50 V, 10%	
C6		Capacitor, Ceramic, 220 pF, 50 V, 10%	
C7	20SA100M	Capacitor, Aluminum, 100 μF, 20 V, 20%	Sanyo
C8		Capacitor, Ceramic, 0.0012 μF, 50 V, 10%	
C9	10SA220M	Capacitor, Aluminum, 220 μF, 10 V, 20%	Sanyo
CR1	50WQ03F	Diode, Schottky, 30 V, 5.5 A	International Rectifier
CR2–4	PMBD914PH	Diode, Switching, 100 V, 200 mA	
L1	T50-26B	Core, Inductor, 27 μH, 27 Turns #22	MicroMetals
Q1	IRF9Z34S	Transistor, MOSFET, p-ch, 60 V, 18A, 0.14 Ω	International Rectifier
Q2	PMBT2222APH	Transistor, NPN, 30 V, 150 mA	
Q3	PMBT2907APH	Transistor, PNP, 40 V, 150 mA	
R1		Resistor, CF, 43 kΩ, 1/4 W, 5%	
R2		Resistor, CF, 51 kΩ, 1/4 W, 5%	
R4		Resistor, CF, 3.0 kΩ, 1/4 W, 5%	
R5		Resistor, MF, 7.50 kΩ, 1/4 W, 1%	
R6		Resistor, MF, 1.87 kΩ, 1/4 W, 1%	
R7		Resistor, CF, 820 Ω, 1/4 W, 5%	
R8		Resistor, CF, 10 kΩ, 1/4 W, 5%	
R9		Resistor, CF, 2.2 kΩ, 1/4 W, 5%	
R10		Resistor, CF, 43 Ω, 1/4 W, 5%	

Table 2. Example 1: Test Results

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	V_I = 12 V, I_O = 0 ~ 3 A	0.4%
Line regulation	I_O = 1.5 A, V_I = 10 ~ 15 V	0.4%
Output ripple (peak-to-peak)	V_I = 12 V, I_O = 3 A	10 mV
Efficiency	V_I = 12 V, I_O = 3 A	81.7%

EXAMPLE 2: 12-V to 3.3-V at 3-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 9. This design is very similar to that in Example 1 and thus much of the detail is not repeated.

Specifications

Input voltage range, V_I . . . . . 10 V to 15 V
Output voltage, V_O . . . . . 3.3 V
Output current, I_O . . . . . 0 A to 3 A
Output ripple voltage . . . . . ≤50 mV
Efficiency . . . . . >70%
Ambient temperature range, T_A . . . . . 0°C to 55°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down (buck) topology operating at 200 kHz.

Duty-Cycle Estimates

Estimate the power-switch duty cycle over the range of input voltages using:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume V_d = 0.6 V)
V_{sat} = power-switch conduction voltage (assume V_{sat} = 0.5 V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for V_I = 10, 12, and 15 V is 0.41, 0.34, and 0.27, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose L1 to limit the peak-to-peak ripple current to 10% of the maximum output current.

$$\Delta I_O = 2 \times 0.1 \times I_{O(max)} = 2 \times 0.1 \times 3 = 0.6 \text{ A peak-to-peak}$$

Inductance is given by:

$$L1 = \left(V_I - V_{sat} - V_O\right) \times D \times \frac{t}{\Delta I_O}$$

Maximum ripple current occurs at the maximum input voltage. Solving for L1:

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)(D)(t)}{\Delta I_O} = \frac{(15 - 0.5 - 3.3)(0.27)\left(5 \times 10^{-6}\right)}{0.6} = 25.2\ \mu H$$

For convenience, use the same inductor as in example 1; therefore, L1 = 27 µH.

Capacitor

Assuming all the inductor ripple current flows through the capacitor and ESR is negligible, calculate the capacitance needed to limit the ripple voltage to 50 mV peak-to-peak.

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.6}{(8)\left(200 \times 10^3\right)(0.05)} = 7.5\ \mu F$$

Assuming the capacitance is at least 10 times greater than the calculated value, the ESR to limit the ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.6} = 83\ m\Omega$$

The rms capacitor-ripple current is:

$$\text{Capacitor current} = 0.289 \times \Delta I_O = 0.289 \times 0.6 = 0.17\ \text{Arms}$$

For convenience, use the same 220-µF, 10-V, 35-mΩ OS-CON SA-series device that was used in Example 1. Alternate choices include a 100-µF, 16-V, 45-mΩ device in the same family but one case-size smaller, and two of the solid tantalum 100-µF, 10-V devices described in example 1.

Power-Switch Design

The power-switch design procedure includes selecting the power switch, the catch rectifier, and the rectifier-snubbing network (if needed), calculating power dissipations and junction temperatures, and ensuring the semiconductors have proper heat sinking.

Power Switch

The surface-mount p-channel device used in Example 1 should work in this design also. The IRF9Z34S has a 60-V drain-to-source breakdown and a 140-mΩ maximum $r_{DS(on)}$ with a 10-V gate drive.

Assume that the worst-case junction temperature is 125°C in a 55°C ambient temperature and the drive circuit provides a 100-ns total switching time (turn-on and turnoff). $r_{DS(on)}$ increases by a factor of 1.6 at 125°C.

$$P_D = \left(3^2\right)(0.14 \times 1.6)(0.41) + (0.5)(10)(3)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)$$

$$P_D = 0.83 + 0.30 = 1.13\ W$$

The thermal impedance $R_{\theta JA}$ = 40°C/W for FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (40 \times 1.13) = 100°C$$

Catch Rectifier

Since the requirements are so similar, consider the same device used in Example 1, the 50WQ03F. The device is a 5.5-A, 30-V Schottky diode in a DPAK, power surface-mount package.

Worst-case dissipation occurs at high line where D is minimum. The 50WQ03F has a maximum forward drop of 0.55 V at a forward current of 3 A and a junction temperature of 125°C.

$$P_D = 3 \times 0.55 \times (1 - 0.39) = 1\ W$$

The thermal impedance $R_{\theta JA}$ = 50°C/W when mounted on FR-4 with 2-oz copper and a one-inch-square pattern.

$$T_J = 55 + (50 \times 1) = 105°C$$

Catch-Rectifier Snubber Network

The capacitor value chosen is 4 to 10 times greater than the rectifier junction capacitance; higher values improve the snubbing but dissipate more power. The 50WQ03F has a typical junction capacitance of 180 pF, and the snubber-capacitor value should be between 750 pF and 1.8 nF. Use C8 = 1.2 nF for convenience. Rectifiers normally ring in the range from 1 to 50 MHz. Choose the snubber resistor, R10, for a 50-ns time constant:

$$R10 = \frac{50 \times 10^{-9}}{C8} = \frac{50 \times 10^{-9}}{1.2 \times 10^{-9}} = 41.7\ \Omega \Rightarrow \text{Use } 43\ \Omega$$

Because the capacitor is charged and discharged each cycle, the power dissipation in R10 is:

$$(2)(C8)\left(V_I{}^2\right)\left(\frac{f_s}{2}\right) = (2)\left(1.2 \times 10^{-9}\right)\left(15^2\right)\left(\frac{200 \times 10^3}{2}\right) = 54 \text{ mW}$$

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, dead-time control voltage, soft-start timing, and short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

Select resistor R1 = 43 kΩ using the graph in Figure 3 to set the oscillator frequency to 200 kHz.

Dead-Time Control

The dead-time-control resistor, R2, is chosen to limit the duty cycle to approximately 0.55, well above the anticipated 0.41 maximum duty cycle. See Figure 4 to find the maximum and minimum ramp-voltage levels, $V_{O(100\%)}$ and $V_{O(0\%)}$. R2 is calculated from the following expression (R_{DT}, R_t in kΩ, D in decimal):

$$R2 = (R1 + 1.25)\left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right]$$

where R1 and R2 are in kΩ.

$$R2 = (43 + 1.25)[0.55\ (1.4 - 0.6) + 0.6] = 46 \text{ k}\Omega \Rightarrow 47 \text{ k}\Omega$$

Soft-Start Timing

As in Example 1, choose C5 = 0.1 μF to bring the output voltage into regulation in approximately 5 ms.

SCP Timing

As in Example 1, choose C4 = 1.0 μF to set the protection enable period to approximately 75 ms.

Output Sense Network

The worst-case input bias current for the TL5001 is 0.5 μA; therefore, the divider current should be approximately 1000 × 0.5 μA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is V_O – 1 V = 2.3 V. Choose R5 = 7.50 kΩ so that the compensation values in Example 1 can be used in this design as well.

$$I_{divider} = \frac{\left(V_O - 1 \text{ V}\right)}{R5} = \frac{3.3 - 1}{7.5 \times 10^3} = 0.307 \text{ mA}$$

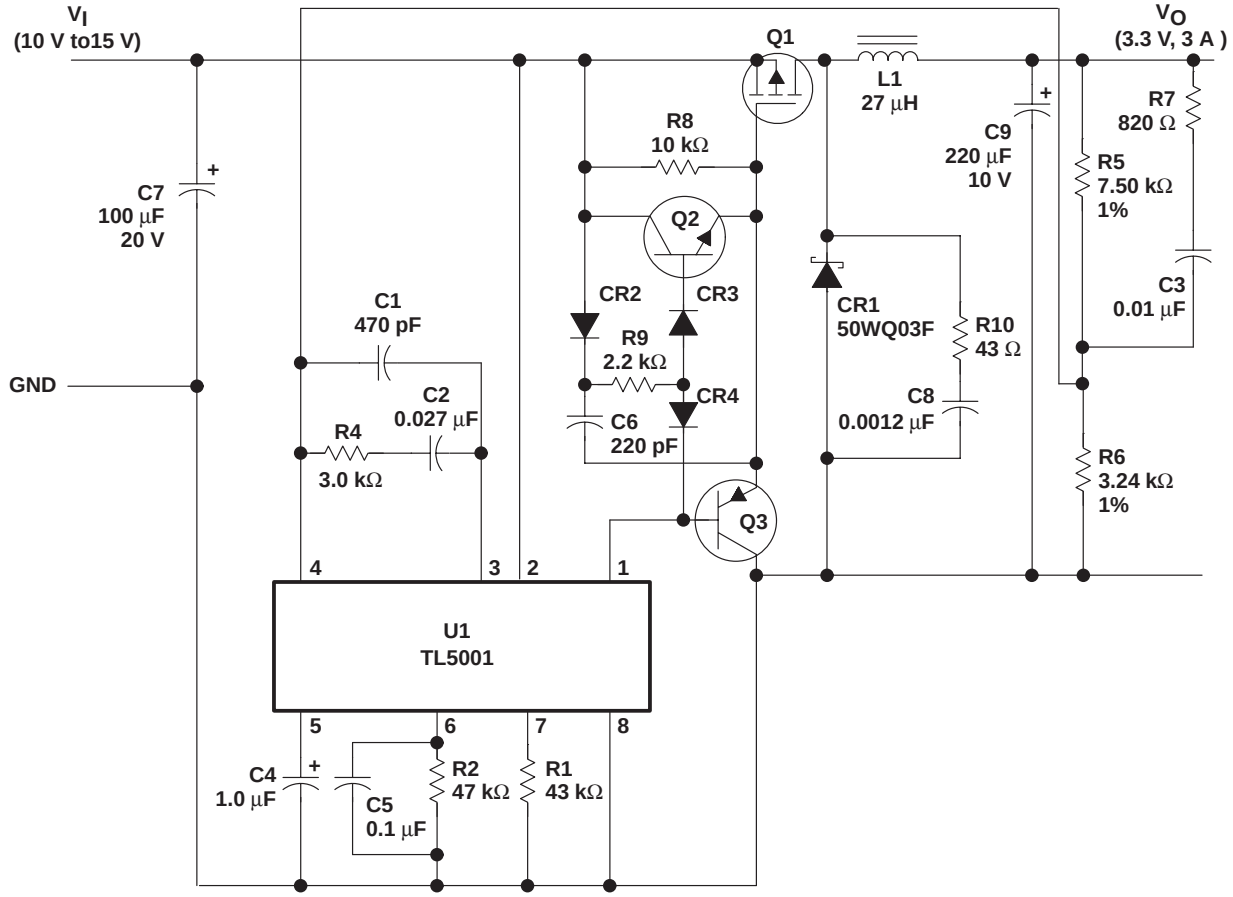
$$R6 = \frac{1 \text{ V}}{0.307 \text{ mA}} = 3.26 \text{ k}\Omega \Rightarrow \text{Use } 3.24 \text{ k}\Omega$$

Loop Compensation

Because the output-filter components, the PWM gain, and R5 are the same as in Example 1, the same compensation design can be used for this application (refer to Example 1 for details).

Summary

The schematic (Figure 9), bill of materials, and test results for the completed design are provided in this summary.



Q1 – IRF9Z34S
Q2 – PMBT2222APH
Q3 – PMBT2907APH
All diodes are PMBD914PH, unless otherwise specified.
R3 – Not used

Figure 9. 12-V to 3.3-V at 3-A Converter

Table 3. Example 2: Bill of Materials

REF DES	PART NO.	DESCRIPTION	MFG
U1	TL5001	IC, PWM Controller	Texas Instruments
C1		Capacitor, Ceramic, 470 pF, 50 V, 10%	
C2		Capacitor, Ceramic, 0.027 μF, 50 V, 10%	
C3		Capacitor, Ceramic, 0.01 μF, 50 V, 10%	
C4		Capacitor, Tantalum, 1.0 μF, 20 V, 10%	
C5		Capacitor, Ceramic, 0.10 μF, 50 V, 10%	
C6		Capacitor, Ceramic, 220 pF, 50 V, 10%	
C7	20SA100M	Capacitor, Aluminum, 100 μF, 20 V, 20%	Sanyo
C8		Capacitor, Ceramic, 0.0012 μF, 50 V, 10%	
C9	10SA220M	Capacitor, Aluminum, 220 μF, 10 V, 20%	Sanyo
CR1	50WQ03F	Diode, Schottky, 30 V, 5.5 A	International Rectifier
CR2–4	PMBD914PH	Diode, Switching, 100 V, 200 mA	
L1	T50-26B	Core, Inductor, 27 μH, 27 Turns #22	MicroMetals
Q1	IRF9Z34S	Transistor, MOSFET, p-ch, 60 V, 18A, 0.14 Ω	International Rectifier
Q2	PMBT2222APH	Transistor, NPN, 30 V, 150 mA	
Q3	PMBT2907APH	Transistor, PNP, 40 V, 150 mA	
R1		Resistor, CF, 43 kΩ, 1/4 W, 5%	
R2		Resistor, CF, 47 kΩ, 1/4 W, 5%	
R4		Resistor, CF, 3.0 kΩ, 1/4 W, 5%	
R5		Resistor, MF, 7.50 kΩ, 1/4 W, 1%	
R6		Resistor, MF, 3.24 kΩ, 1/4 W, 1%	
R7		Resistor, CF, 820 Ω, 1/4 W, 5%	
R8		Resistor, CF, 10 kΩ, 1/4 W, 5%	
R9		Resistor, CF, 2.2 kΩ, 1/4 W, 5%	
R10		Resistor, CF, 43 Ω, 1/4 W, 5%	

Table 4. Example 2: Test Results

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	V_I = 12 V, I_O = 0 ~ 3 A	0.7%
Line regulation	I_O = 1.5 A, V_I = 10 ~ 15 A	0.9%
Output ripple (peak-to-peak)	V_I = 12 V, I_O = 3 A	8 mV
Efficiency	V_I = 12 V, I_O = 3 A	74.7%

EXAMPLE 3: 5-V to 3.3-V at 0.75-A STEP-DOWN CONVERTER

Design Criteria

The schematic of the final design is provided in Figure 13 . Example 1 gives a more detailed explanation of the same design procedure used in this section.

Specifications

Input voltage range, V_I	4.75 V to 5.25 V
Output voltage, V_O	3.3 V
Output current, I_O	0 A to 0.75 A
Output ripple voltage	≤50 mV
Regulation	1%
Efficiency	>70%
Ambient temperature range, T_A	−20°C to 65°C

Surface-mount components should be employed wherever feasible. The dc/dc converter is implemented with a continuous-mode, fixed-frequency-PWM step-down (buck) converter operating at 200 kHz.

Duty-Cycle Estimates

Estimate the power-switch duty cycle over the range of input voltages using:

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

Where

V_d = catch-rectifier conduction voltage (assume V_d = 0.5 V)
V_{sat} = power-switch conduction voltage (assume V_{sat} = 0.25 V)

The results can be recalculated if actual values are too far from the initial estimate.

The duty cycle for V_I = 4.75, 5, and 5.25 V is 0.84, 0.80, and 0.76, respectively.

Output Filter

The output filter is a single-stage LC design.

Inductor

Choose L1 to maintain continuous-mode operation to 20% of the rated output current.

$$\Delta I_O = 2 \times 0.2 \times I_{O(max)} = 2 \times 0.2 \times 0.75 = 0.3 \text{ A peak-to-peak}$$

The inductor value is calculated using

$$L1 = \frac{\left(V_I - V_{sat} - V_O\right)DTs}{\Delta I_O}$$

where Ts is the period of the converter operating frequency.

Maximum ripple current occurs at the maximum input voltage. Solving for L1:

$$L1 = \frac{(5.25 - 0.25 - 3.3)(0.76)\left(5 \times 10^{-6}\right)}{0.3} = 21.5 \text{ µH}$$

Use L1 = 20 µH (Coiltronics CTX20-1, 1.15 A dc-current rating, surface-mount package). Using the new value for L1, ΔI_O is recalculated:

$$\Delta I_O = \frac{\left(V_I - V_{sat} - V_O\right)DTs}{L1} = \frac{(5.25 - 0.25 - 3.3)(0.76)\left(5 \times 10^{-6}\right)}{20 \times 10^{-6}} = 323 \text{ mA peak-to-peak}$$

Capacitor

Assuming all the inductor ripple current flows through the capacitor and ESR is zero, the capacitance needed to limit the ripple voltage to 50 mV peak-to-peak is:

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.323}{(8)\left(200 \times 10^3\right)(0.05)} = 4.04\ \mu F$$

If the capacitance is at least ten times greater than the calculated value, the ESR to limit the ripple to 50 mV peak-to-peak is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.323} = 155\ m\Omega$$

Capacitor ripple current is seldom a problem in low-voltage converters unless a large number of devices are paralleled. However, the capacitor current is calculated as follows:

$$I_{rms} = 0.289 \times \Delta I_O = 0.289 \times 0.323 = 0.093\ \text{Arms}$$

The output filter capacitor(s) should provide at least ten times the calculated minimum capacitance and an ESR 30% to 50% lower than the calculated maximum to provide some margin for ESL, PCB leads, temperature, and aging. The 200-kHz, 85°C ripple current should be 0.25 Arms or greater, and the voltage rating should be at least 6.3 V.

For this case, a 100-µF, 10-V tantalum electrolytic with an ESR of 0.100 Ω maximum was chosen.

Power-Switch Design

The power-switch design procedure includes selecting the power switch, the catch rectifier, and the rectifier-snubbing network (if needed); calculating power dissipations and junction temperatures; and ensuring the semiconductors have proper heat sinking.

Power Switch

This design uses a p-channel MOSFET to simplify the drive-circuit design and minimize component count. Based on the preliminary estimate, $r_{DS(on)}$ should be less than 0.25 V ÷ 0.75 A = (333 mΩ) with a 5-V gate drive and a drain-to-source breakdown voltage appropriate for a 5-V supply. A low gate-to-source threshold voltage and surface-mount packaging are also desirable.

The TPS1101D is a 15-V p-channel MOSFET in an SO-8 package with $r_{DS(on)}$ = 0.19 mΩ maximum, with a 4.5-V gate drive.

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

Where t_{r+f} = total MOSFET switching time (turn-on and turnoff) and $r_{DS(on)}$ is adjusted for temperature. Assuming the drive circuit is adequate for t_{r+f} = 100 ns and the junction temperature is 100°C with a 65°C ambient, the adjustment factor is 1.3 and $r_{DS(on)} = 1.3 \times 0.19 = 0.25$.

$$P_D = \left[\left(0.75^2\right)(0.25)(0.80)\right] + \left[(0.5)(5)(0.75)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)\right]$$

$$P_D = 113 + 38 = 151\ mW$$

The thermal impedance $R_{\theta JA}$ = 158°C/W for FR-4 with no special heat-sinking considerations.

$$T_J = T_A + (R_{\theta JA} \times P_D) = 65 + (158 \times 0.151) = 89°C$$

Catch Rectifier

The power dissipation in this design is very low because of a relatively low output-current requirement and the high-power-switch duty cycles. Consequently, a small surface-mount Schottky device such as the MBRS140T3 is more than adequate. The MBRS140T3 is rated for 1 A of forward current and a 40-V breakdown. The conduction drop, V_d, is 0.35-V at 1-A forward current and a 100°C junction. The power dissipation is:

$$P_D = I_O \times V_d \times (1 - D)$$

$$P_D = 0.75 \times 0.35 \times (1 - 0.76) = 63 \text{ mW}$$

In the absence of thermal-impedance data for this package with FR-4 mounting, a reasonable estimate of junction temperature is not practical. However, some assurance can be derived from considering the thermal impedance necessary to limit the junction to 100°C which is comfortably below the 125°C maximum rating. The thermal impedance, $R_{\theta JA}$, needed to raise the junction temperature from the 65°C ambient to 100°C with 63 mW of dissipation is:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} = \frac{100 - 65}{0.063} = 556°C/W$$

There should be no problem since even signal diodes are in the 300°C to 400°C/W range. Some preliminary testing to establish thermal performance is highly recommended for applications where the margins are lower.

Controller Design

The controller-design procedure involves choosing the components required to program the TL5001 and includes setting the oscillator frequency, dead-time control voltage, soft-start timing, and short-circuit-protection timing. The sense-divider network and loop-compensation designs are also addressed in this section.

Oscillator Frequency

From the graph in Figure 3, choose R2 = 43 kΩ to set the oscillator frequency to 200 kHz.

Dead-Time Control

The maximum duty cycle in this application is 84% and because there is no benefit in limiting the duty cycle a few points below 100%, the dead-time control resistor is omitted.

Soft-Start Timing

The DTC input can be used to soft start the converter even though dead-time control is not implemented. The soft-start capacitor is charged with a constant current approximately equal to the current flowing from the RT terminal. The output voltage should be in regulation by the time C5 has charged to 1.4 V. Choose C5 such that the output voltage comes up in 6 ms.

$$\text{Charging current} = \frac{1 \text{ V}}{43 \text{ k}\Omega} = 23.3 \text{ μA}$$

$$C5 = \frac{\left(23.3 \times 10^{-6}\right)\left(6 \times 10^{-3}\right)}{1.4} = 0.1 \text{ μF}$$

SCP Timing

As in Example 1, choose C4 = 1 μF to set the protection enable period to approximately 75 ms.

Output Sense Network

The worst-case input bias current for TL5001 is 0.5 μA; therefore, the divider current should be approximately 1000 × 0.5 μA = 0.5 mA. In regulation, the voltage across R6 is 1 V and the voltage across R5 is V_O – 1 V = 2.3 V. For this design, R5 is set at 7.50 kΩ.

$$I_{divider} = \frac{\left(V_O - 1 \text{ V}\right)}{R5} = \frac{3.3 - 1}{7.5 \times 10^3} = 0.307 \text{ mA}$$

$$R6 = \frac{1 \text{ V}}{0.307 \text{ mA}} = 3.26 \text{ k}\Omega \Rightarrow \text{Use } 3.24 \text{ k}\Omega$$

Loop Compensation

Refer to Example 1 for more detailed explanation.

The open-loop response without the error amplifier consists of the gain of the PWM/power switch, A_{PWM}, and the output filter response. The gain, A_{PWM}, is:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{(5 - 0)}{(1.4 - 0.6)} = 6.25 \Rightarrow 15.9 \text{ dB at nominal input}$$

Similarly, the gain is 15.5 dB at low line and 16.3 dB at high line.

The output filter produces an underdamped complex-pole pair at the filter's resonant frequency, and the capacitor ESR puts a zero in the response above the resonant frequency. The complex poles are located at:

$$\frac{1}{2\ \pi\ \sqrt{LC}} = \frac{1}{2\ \pi\ \sqrt{\left(20 \times 10^{-6}\right)\left(100 \times 10^{-6}\right)}} = 3.56 \text{ kHz}$$

The zero is located at:

$$\frac{1}{2\pi\ R_S C} = \frac{1}{(2\pi)(0.1)\left(100 \times 10^{-6}\right)} = 15.9 \text{ kHz.}$$

Figure 10 includes gain and phase plots of the open-loop response (error amplifier not included) obtained from a simple SPICE simulation.

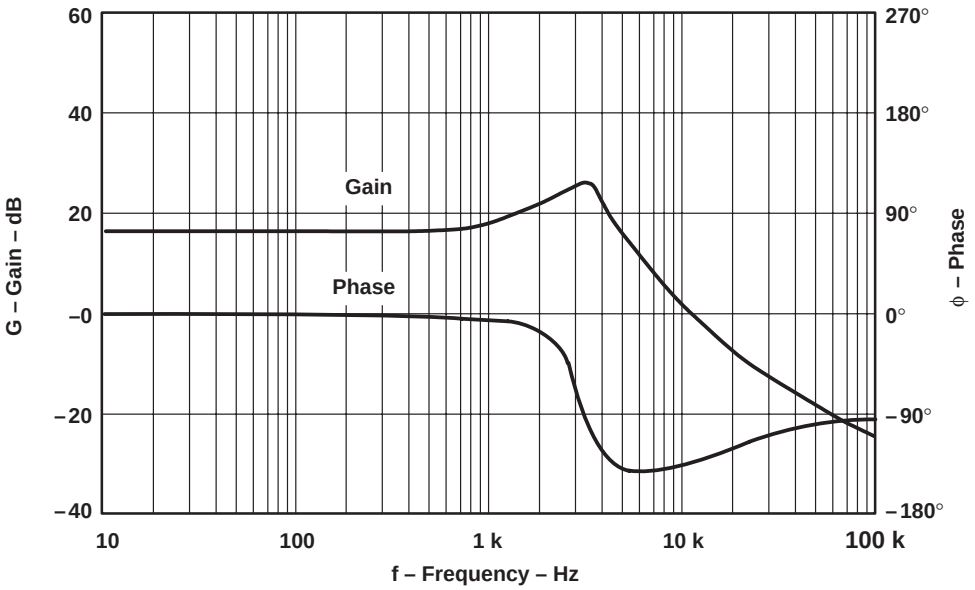


Figure 10. Uncompensated Open-Loop Response

Choose a unity-gain frequency of approximately 20 kHz to provide good transient response. Figure 11 shows a standard compensation network chosen for this example.

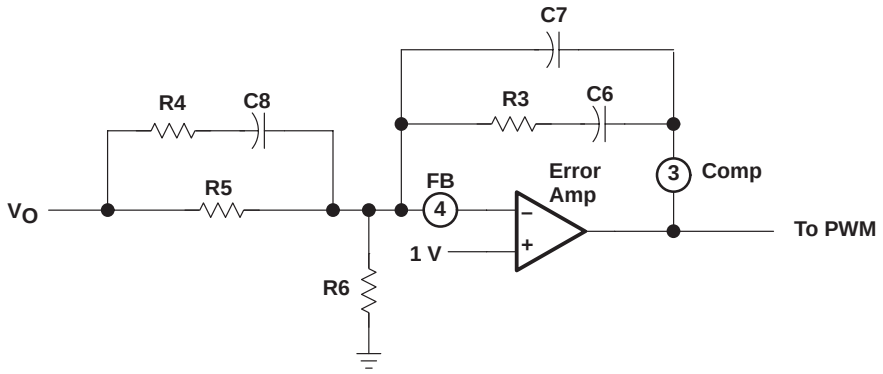


Figure 11. Compensation Network

Assuming an ideal amplifier, the transfer function is:

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C6 + C7)}\right]\left[\frac{[S(R5 + R4)\ C8 + 1]\ (S\ R3\ C6 + 1)}{(S\ R4\ C8 + 1)\ \left[S\ R3\ \left(C6 \parallel C7\right) + 1\right]}\right]$$

The integrator gain, 1/[R5 · (C6 + C7)], is used to set the open-loop unity-gain frequency. The zeros are located at approximately the same frequency as the output-filter poles to compensate for the gain reduction and phase shift. The pole at 1/(2π · R4 · C8) is positioned at approximately the same frequency as the zero in the output filter to maintain the 20 dB-per-decade roll-off in the gain response. The final pole at 1/(2π · R3 · C6 || C7) is placed between half the operating frequency and the operating frequency to minimize noise at the pulse-width-modulator input.

The sum of the gains of the modulator, the LC filter, and the error amplifier is 0 dB at the unity-gain frequency. The gain of the modulator/LC filter at 20 kHz may be calculated or obtained from a bode plot using straight-line approximations or from a simple SPICE simulation. As shown in Figure 10, the modulator/LC filter gain is –8 dB at 20 kHz.

The compensation network has two zeros at 3.6 kHz to cancel out the LC filter poles. These two zeros contribute a gain of 29 dB at 20 kHz; therefore, the gain contributed by the compensation-network integrator needs to be –21 dB [0 – (–8 + 29) = –21]. The integrator gain of –21 dB translates to a voltage gain of 0.089.

$$\frac{1}{(2\pi)\left(f_T\right)(R5)(C6 + C7)} = 0.089\ \left(\text{at } f_T = 20\ \text{kHz}\right)$$

$$C6 = \frac{1}{(2\pi)\left(f_T\right)(R5)(0.089)} = \frac{1}{(6.28)\left(20 \times 10^3\right)\left(7.5 \times 10^3\right)(0.089)} = 0.0119\ \mu F \Rightarrow \text{Use } C6 = 0.012\ \mu F.$$

R3 is chosen to position a zero at 3.6 kHz.

$$R3 = \frac{1}{(2\pi)(f)(C6)} = \frac{1}{(6.28)\left(3.6 \times 10^3\right)\left(0.012 \times 10^{-6}\right)} = 3.69\ k\Omega \Rightarrow \text{Use } 3.6\ k\Omega$$

R4 and C8 are chosen to provide an additional zero, f_Z, at 3.6 kHz and a pole, f_P, at 15.9 kHz.

$$C8 = \frac{\frac{1}{f_Z} - \frac{1}{f_P}}{(2\pi)(R5)} = \frac{\left[\frac{1}{3.6 \times 10^3} - \frac{1}{15.9 \times 10^3}\right]}{(6.28)\left(7.5 \times 10^3\right)} = 0.0046\ \mu F \Rightarrow \text{Use } C8 = 0.0047\ \mu F$$

$$R4 = \frac{1}{(2\pi)\left(f_P\right)(C8)} = \frac{1}{(6.28)\left(15.9 \times 10^3\right)\left(0.0047 \times 10^{-6}\right)} = 2.13\ k\Omega \Rightarrow \text{Use } 2.0\ k\Omega$$

C7 is chosen to provide the pole at 100 kHz. Assuming C6 >> C7,

$$C7 = \frac{1}{(2\pi)\left(f_p\right)(R3)} = \frac{1}{(6.28)\left(100 \times 10^3\right)(3600)} = 442\ pF \Rightarrow \text{Use } 470\ pF$$

Results of the compensated-system response are shown in Figure 12.

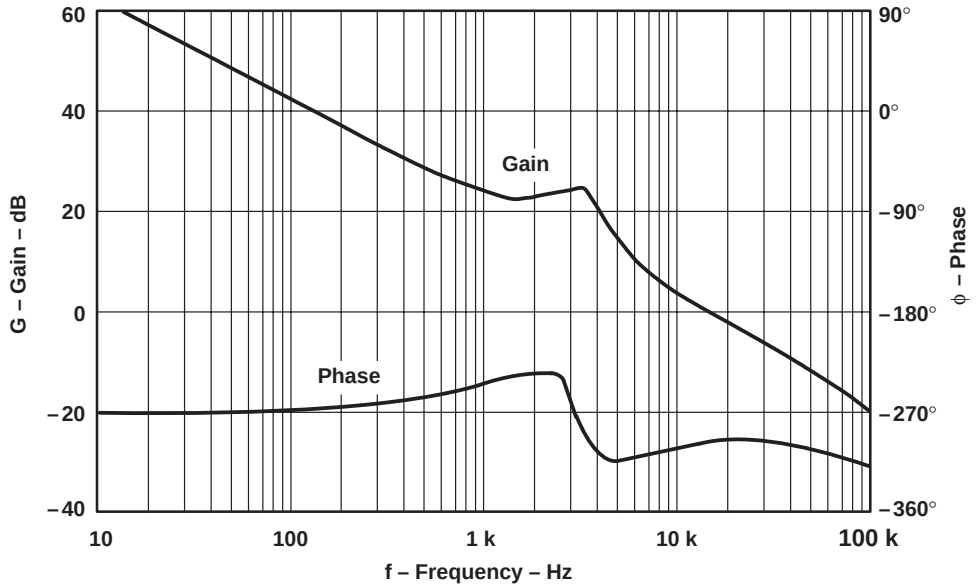
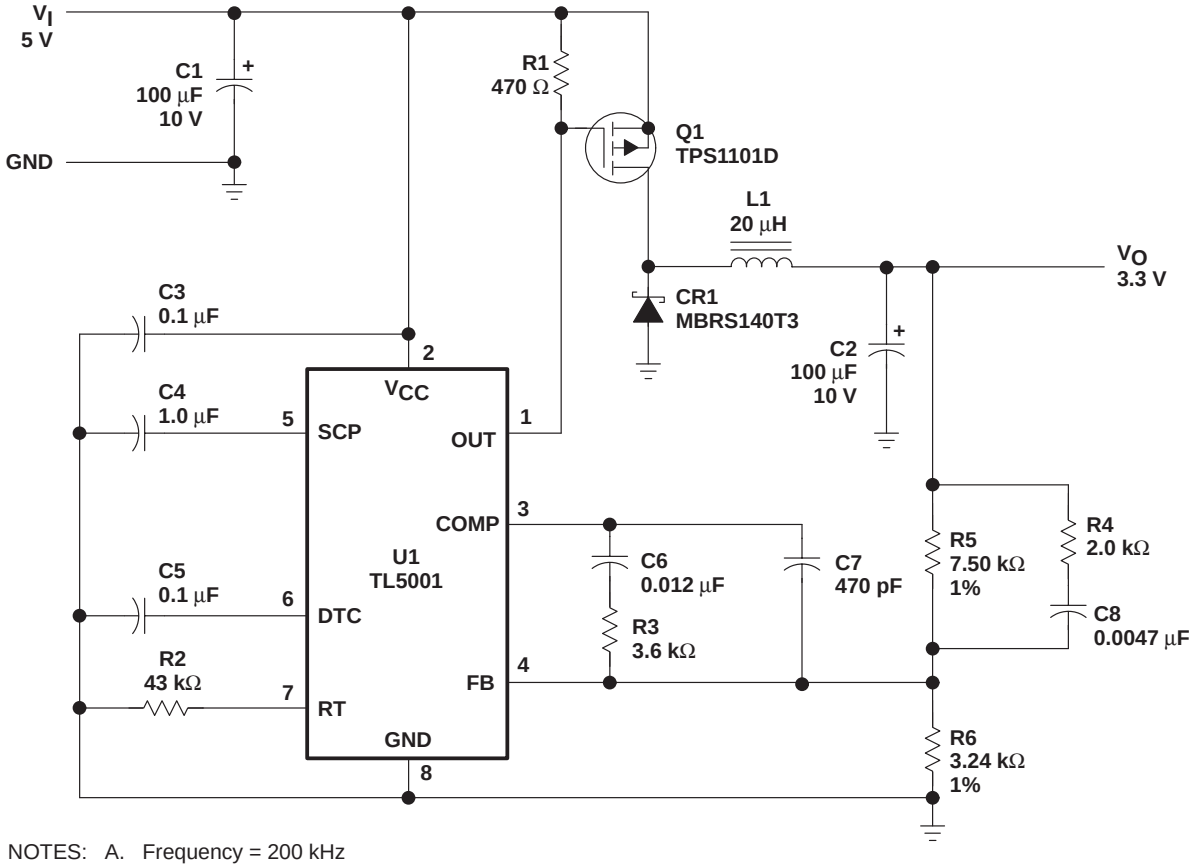


Figure 12. Compensated-Loop Response

Summary

The schematic (Figure 13), bill of materials, and test results for the completed design are provided in this summary.



NOTES: A. Frequency = 200 kHz
B. Duty cycle = 100% MAX
C. Soft-start timing = 6 ms
D. SCP timing = 75 ms

Figure 13. 5-V to 3.3-V/0.75-A Converter

Table 5. Example 3: Bill of Materials

REF DES	PART NO.	DESCRIPTION				MFG
U1	TL5001	IC, PWM Controller				Texas Instruments
C1, C2	TPSD107M010R0100	Capacitor, Tantalum,	100 μF,	10 V,	20%	AVX
C4		Capacitor, Ceramic,	1.0 μF,	50 V,	10%	
C3, C5		Capacitor, Ceramic,	0.1 μF,	50 V,	10%	
C6		Capacitor, Ceramic,	0.012 μF,	50 V,	10%	
C7		Capacitor, Ceramic,	470 pF,	50 V,	10%	
C8		Capacitor, Ceramic,	0.0047 μF,	50 V,	10%	
CR1	MBRS140T3	Diode, Schottky,	20 V,	1 A		Motorola
L1	CTX20-1	Inductor, Toroid,	20 μH			Coiltronics
Q1	TPS1101D	Transistor, MOSFET,	p-ch,	15 V,	0.19 Ω	Texas Instruments
R1		Resistor, CF,	470 Ω,	1/4 W,	5%	
R2		Resistor, CF,	43 kΩ,	1/4 W,	5%	
R3		Resistor, CF,	3.6 kΩ,	1/4 W,	5%	
R4		Resistor, CF,	2.0 kΩ,	1/4 W,	5%	
R5		Resistor, MF,	7.50 kΩ,	1/4 W,	1%	
R6		Resistor, MF,	3.24 kΩ,	1/4 W,	1%	

Table 6. Example 3: Test Results

PARAMETER	TEST CONDITIONS			MEASUREMENT
Load regulation	V_I = 5 V,	I_O = 0 ~ 750 mA		1.4%
Output ripple (peak-to-peak)	I_O = 750 mA			< 20 mV
Efficiency	V_I = 5 V,	I_O = 750 mA,	Q1 = SI9405	74.4%
	V_I = 5 V,	I_O = 750 mA,	Q1 = TPS1101	84.1%†

† The higher efficiency achieved with the TPS1101 is due to lower gate capacitance, which speeds up switching and reduces switching loss.

Appendix A
5-V Prototype-Board Waveforms

The following photos were taken using the 12-V to 5-V prototype breadboard that was designed and documented as presented in the first section of this application report. The results are typical of those seen on the other designs in this paper.

Minimum Dead Time (maximum duty cycle)

The dead time of the output switch was measured with the feedback resistance disconnected.

Vertical: 2 V/div
Horizontal: 1 μs/div
Coupling: dc

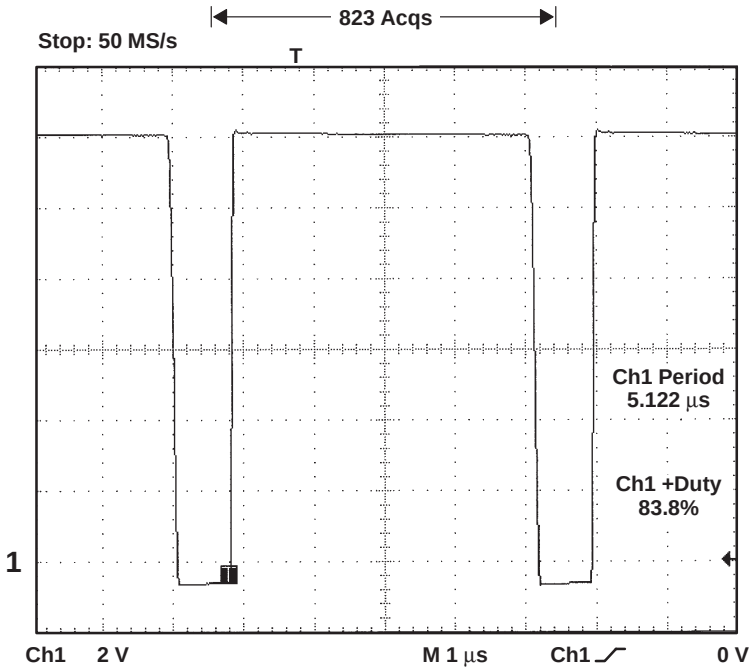


Figure A–1

Output Switch Drain to Ground Voltage

The input of the low-pass output filter is shown in Figure A–2. The high-level voltage is equal to the input voltage minus $V_{DS(on)}$. The low-level voltage is one diode drop below ground.

Vertical: 2 V/div
Horizontal: 1 μs/div
Coupling: dc

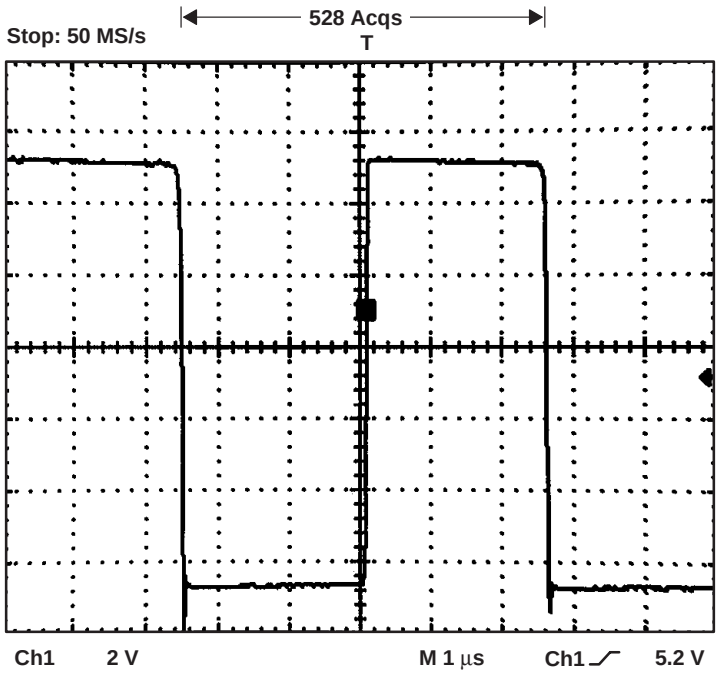


Figure A–2

Output Voltage Rise Time (electronic load)

The soft-start circuit slows the rise of the output voltage to prevent excessive overshoot.

Vertical: 1 V/div
Horizontal: 2 ms/div
Coupling: dc

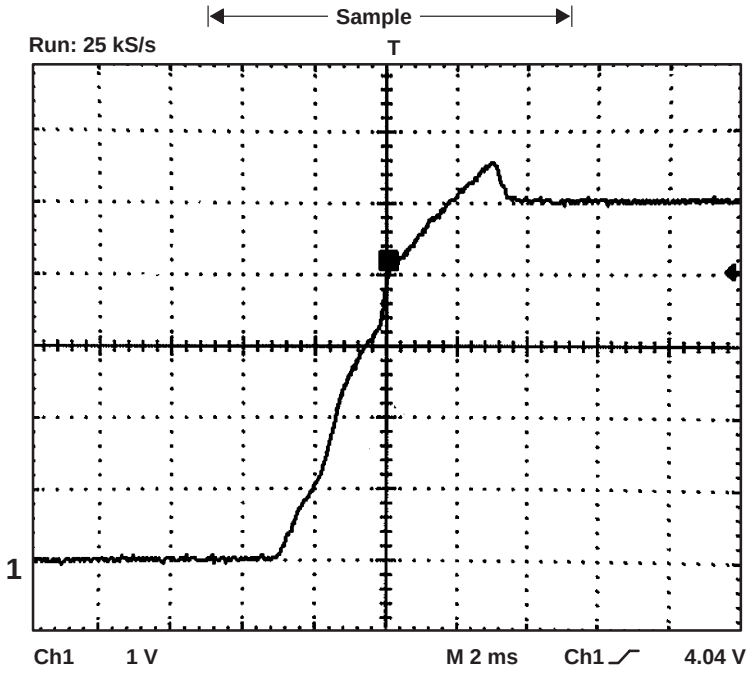


Figure A–3

Output Voltage Rise Time (resistive load)

This photo shows the response to a resistive load.

Vertical: 1 V/div
Horizontal: 2 ms/div
Coupling: dc

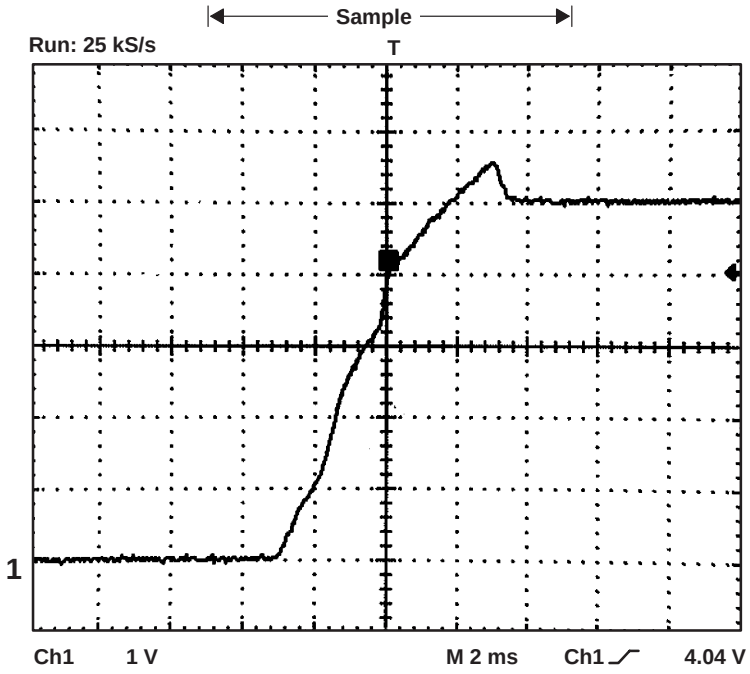


Figure A–4

Output Voltage Ripple

The output ripple is shown in Figure A–5. The triangular-shaped ripple is clearly a function of the ESR of the output capacitor.

Vertical: 2 mV/div
Horizontal: 2 μs/div
Coupling: ac

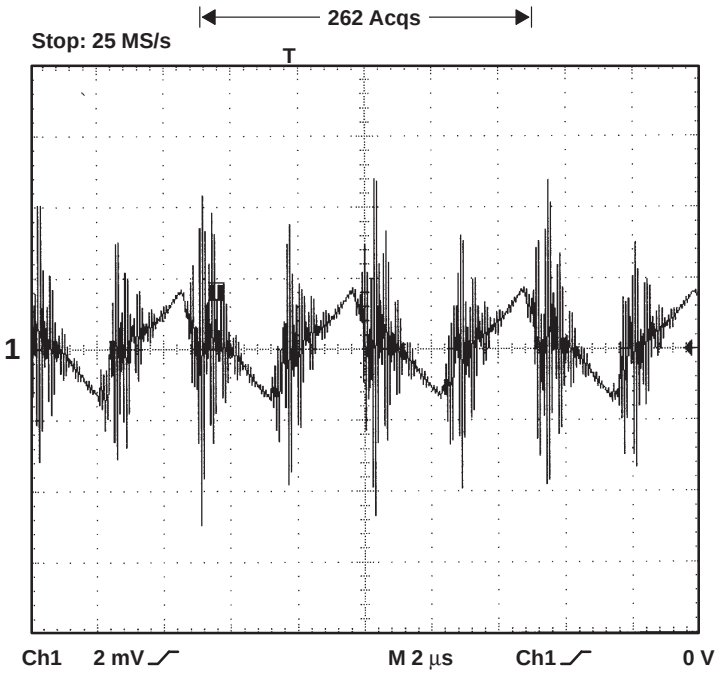


Figure A–5

Output Dynamic Response

The response of the output to step-load changes is shown in Figure A–6. The electronic load was stepped from 1.5 A to 3 A.

Top Waveform: V_O
- Vertical: 100 mV/div
- Horizontal: 0.5 ms/div
- Coupling: ac

Bottom Waveform: I_O
- Vertical: 1 A/div
- Horizontal: 0.5 ms/div
- Coupling: dc

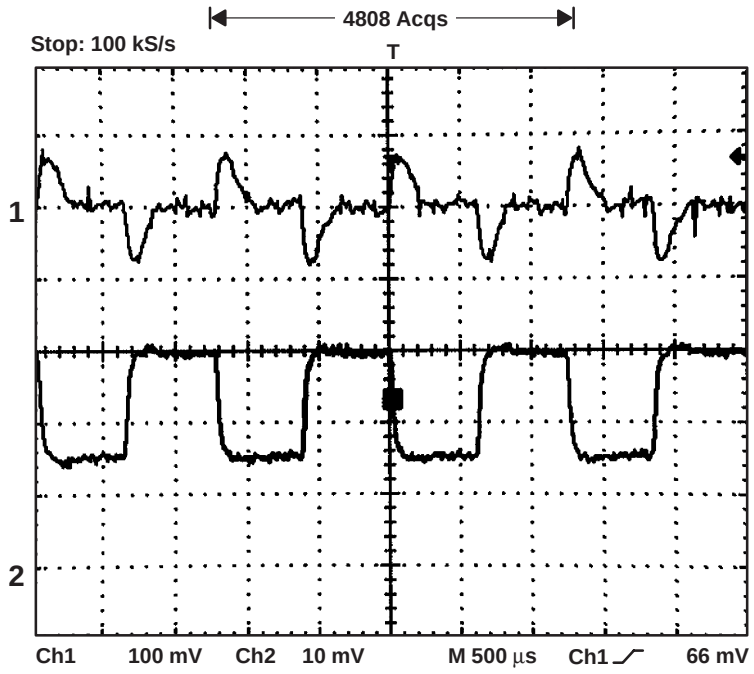


Figure A–6

Acknowledgement

This application report is the synergistic result of many individual efforts. The work involved included characterization of the controller chip; design, breadboarding, and debugging of application examples; and preparation of the report itself. Every effort has been made to provide a document that is useful and understandable to the customer/designer. The following list, though not all inclusive, represents the major contributors to this document:

Co-authors and Engineering

Bill Johnston, Power Supply Systems Engineering Manager
Philip Rogers, Power Supply Systems Engineer
John Vincent, Vincent Enterprises, Consultant

Documentation

Ron Eberhart, Technical Writer
Fran Caldwell, Publications Specialist/Formatter
Jim Schrader, Technical Illustrator

Proofreading and Suggestions

Kazu Kudoh, Product Specialist
Jeff Hooker, Product Specialist
Bob Newton, Product Specialist
Rob Saunier, Applications Engineer

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