Introduction

Recent growth in high-speed data transmission between high-speed ICs demand more bandwidth than ever before while still maintaining high performance, low power consumption and good noise immunity. Emitter Coupled Logic (ECL) recognized the challenge and provided high performance and good noise immune devices. ECL migrated toward low voltages to reduce the power consumption and to keep up with current technology trends by offering 3.3 V and 2.5 V Low Voltage ECL (LVECL) devices. LVECL devices working off the positive 3.3 V or 2.5 V supply voltages are called the Low Voltage Positive ECL (LVPECL). LVPECL maintains 750 mV output swing with a 0.9 V offset from VCC, which makes them ideal as peripheral components.

LVDS (Low Voltage Differential Signaling) technology also addresses the needs of current high performance applications. LVDS as specified in ANSI/TIA/EIA-644 by Data Transmission Interface committee TR30.2 and IEEE 1596.3 SCI-LVDS by IEEE Scalable Coherent Interface standard (SCI) is a high speed, low power interface that is a solution in many application areas. LVDS provides an output swing of 250 mV to 400 mV with a DC offset of 1.2 V. External resistor components are required for board-to-board data transfer or clock distribution.

LVPECL and LVDS are both differential low voltage signals, but with different amplitude and different offset. The purpose of this documentation is to show the interfacing between ECL and LVDS. In addition, it gives interface suggestions to and from 5.0 V supplied PECL devices and negative supplied ECL or NECL levels

ECL levels

Today’s applications typically use ECL devices in the PECL mode. PECL (Positive ECL) is nothing more than supplying any ECL device with a positive power supply \( V_{CC} = +5.0 \text{ V}, V_{EE} = 0 \text{ V} \). In addition, ECL uses differential data transmission technology, which results in better noise immunity. Since the common mode noise is coupled onto the differential interconnect, it will be seen as a common mode modulation and will be rejected.

With the trend towards low voltage systems, a new generation of ECL circuitry has been developed. The Low Voltage NECL (LVPECL) devices work using negative \(-3.3 \text{ V} \) or \(-2.5 \text{ V} \) power supply, or more popular positive power supplies, \( V_{CC} = +3.3 \text{ V} \) or \(+2.5 \text{ V} \) and \( V_{EE} = \text{GND} \) as LVPECL.

The temperature compensated (100EL, 100LVEL, 100EP, 100LVEP) output DC levels for the different supply levels are shown in Table 1. ECL outputs are designed as an open emitter, requiring a DC path to a more negative supply than \( V_{OL} \). A pull down resistor termination can be used to terminate the transmission line (see AND8020 for ECL Termination information).

ECL standard DC input levels are also relative to \( V_{CC} \). Many devices are available with Voltage Input HIGH Common Mode Range (\( V_{IHCMR} \)). These differential inputs allow processing signals with small swings (down to 200 mV, 150 mV or even 50 mV signal levels) within an appropriate offset range. The \( V_{IHCMR} \) ranges of ECL devices are listed in each respective data sheets.
Table 1. MC100EXXX/MC100ELXXX/LVELXXX/EPXXX/LVEPXXX (\(T_A = 0^\circ C\) to +85°C)

| Symbol | Parameter | Parameter | Parameter | Parameter | Parameter
|--------|-----------|-----------|-----------|-----------|-----------
|        | 2.5 V LVPECL (Note 1) | 3.3 V LVPECL (Note 1) | 5.0 V PECL (Note 1) | NECL | Unit |
| VCC    | +2.5 | +3.3 | +5 | GND | V |
| VEE    | GND | GND | GND | -5.2, -4.5, -3.3 or -2.5 | V |
| VOH    | Maximum Output HIGH Level | 1.680 | 2.480 | 4.180 | -0.820 | V |
| VOH    | Typical Output HIGH Level | 1.555 | 2.355 | 4.055 | -0.945 | V |
| VOH    | Minimum Output HIGH Level | 1.430 | 2.230 | 3.930 | -1.070 | V |
| VOL    | Maximum Output LOW Level | 0.880 | 1.680 | 3.380 | -1.620 | V |
| VOL    | Typical Output LOW Level | 0.755 | 1.555 | 3.255 | -1.745 | V |
| VOL    | Minimum Output LOW Level | 0.630 | 1.430 | 3.130 | -1.870 | V |

1. All levels vary 1:1 with VCC

LVDS Levels

As the name indicates, the LVDS main attribute is the low voltage amplitude levels compared to other data transmission standards, as shown in Figure 1. The LVDS specification states 250 mV to 400 mV output swing for driver/transmitter (Vpp). The low voltage swing levels result in low power consumption while maintaining high performance levels required by most users. In addition, LVDS uses differential data transmission technology equivalent to ECL. Furthermore, LVDS technology is not dependent on specific power supply levels like ECL technology. This signifies an easy migration path to lower supply voltages such as 3.3 V, 2.5 V, or lower voltages while still maintaining the same signaling levels and high performance. ON Semiconductor currently provides a 2.5 V 1:5 dual differential LVDS Clock Driver/Receiver (MC100EP210S).

LVDS require a 100 Ω load resistor between the differential outputs to generate the Differential Output Voltage (VOD) with a maximum current of 2.5 mA flowing through the load resistor. This load resistor will terminate the 50 Ω controlled characteristic impedance line, which prevent reflections and reduces unwanted electromagnetic emission (Figure 2).

![Figure 2. LVDS Output Definition](image)

LVDS receivers require 200 mV minimum input swing within the input voltage range of 0 V to 2.4 V and can tolerate a minimum of ±1.0 V ground shift between the driver’s ground and the receiver’s ground, since LVDS receivers have a typical driver offset voltage of 1.2 V. The common mode range of the LVDS receiver is 0.2 V to 2.2 V, and the recommended LVDS receiver input voltage range is from 0 V to 2.4 V. Common mode range of LVDS is similar to the theory of Voltage Input HIGH Common Mode Range (\(V_{IHCMR}\)) of ECL devices.

Currently more LVDS standards are being developed as LVDS technology gains in popularity.
**BLVDS**

National Semiconductor developed Bus LVDS (BLVDS) for multipoint applications. This standard is targeted at heavily loaded back planes, which reduces the impedance of the transmission line by 50% or more. By providing increased drive current, the double termination seen by the driver will be compensated.

**M-L VDS**

TIA TR30.2 standards group is developing another multipoint LVDS application called Multipoint LVDS (M-LVDS). The maximum data rate is 500 Mbps.

**GLVDS and SLVS**

Ground referenced LVDS (GLVDS) is similar to LVDS except the driver output voltage offset is nearer to ground. The advantage of GLVDS is the use of very low power supply voltages (0.5 V).

Similar standard to GLVDS is SLVS (Scalable Low-Voltage Signaling for 400 mV) by JEDEC. The interface is terminated to ground with 400mV swing and a minimum supply voltage of 0.8 V.

**LVDM**

Texas Instruments developed LVDM, which is designed for double 100 Ω-terminated applications. The driver’s output current is two times the standard LVDS, thus producing LVDS characteristic levels.

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### Table 2. LVDS LEVELS

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>V&lt;sub&gt;PP&lt;/sub&gt;</td>
<td>Output Differential Voltage</td>
<td>250</td>
<td>400</td>
<td>240</td>
<td>500</td>
<td>480</td>
<td>650</td>
<td>150</td>
</tr>
<tr>
<td>V&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Output Offset Voltage</td>
<td>1125</td>
<td>1275</td>
<td>1225</td>
<td>1375</td>
<td>300</td>
<td>2100</td>
<td>75</td>
</tr>
<tr>
<td>R&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Output Offset Voltage</td>
<td>100</td>
<td>27</td>
<td>50</td>
<td>50</td>
<td>Internal To Rx</td>
<td>50</td>
<td>W</td>
</tr>
<tr>
<td>I&lt;sub&gt;OD&lt;/sub&gt;</td>
<td>Output Differential Current</td>
<td>2.5</td>
<td>4.5</td>
<td>9</td>
<td>17</td>
<td>9</td>
<td>13</td>
<td>Adjustable</td>
</tr>
</tbody>
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**Transmitter**

**Receiver**

Common mode range inputs are capable of processing differential signals with 150 mV to 400 mV amplitude. The ECL input processes signals up to 1.0 V amplitude. The DC voltage levels should be within the voltage input HIGH common mode range (V<sub>IHCMR</sub>).

To interface between these 2 voltage levels, capacitive coupling can be used. Only clock or coded signals should be capacitively coupled. A capacitive coupling of NRZ signals will cause problems, which can require a passive or active interfacing.
Capacitive Coupling LVDS to ECL Using \( V_{BB} \)

Several ECL devices provide a \( V_{BB} (V_{BB} = V_{CC} - 1.3V) \) reference voltage. It can be used for differential capacitive coupling. The \( V_{BB} \) needs to be decoupled to GND via a 10 nF capacitor. (Figure 3)

![Figure 3. Capacitive Coupling LVDS to ECL Using \( V_{BB} \)](image)

Capacitive Coupling LVDS to ECL with External Biasing

If \( V_{BB} \) reference voltage is not available, equivalent DC voltage can be generated using a resistor divider network. The resistor values depend on \( V_{CC} \) and \( V_{EE} \) voltages (Table 3). Stability is enhanced during null signal conditions if a 50 mV differential voltage is maintained between the divider networks. (Figure 4)

### Table 3. Examples:

| \( V_{CC} \) = GND | \( V_{EE} \) = -5.0 V | R1 = 1.2 kΩ | R2 = 3.4 kΩ |
| \( V_{CC} \) = GND | \( V_{EE} \) = -3.3 V | R1 = 680 | R2 = 1.0 kΩ |
| \( V_{CC} \) = GND | \( V_{EE} \) = -2.5 V | R1 = 100 | R2 = 90 |

![Figure 4. Capacitive Coupling LVDS to ECL with External Biasing](image)

In the layout for both interfaces, the resistors and the capacitors should be located as close as possible to the ECL input to insure reduced reflection and increased signal integrity.

Capacitive Coupling ECL to LVDS

The ECL output requires a DC current path to \( V_{EE} \); therefore, the pulldown termination resistors, \( R_T \), are connected to \( V_{EE} \). The Thevenin resistor pair represent the termination of the transmission line \( Z = R_1 || R_2 \) and generates an appropriate DC offset level of 1.2 V. (Figure 5)

![Figure 5. Capacitive Coupling ECL to LVDS](image)

An example of capacitive coupled LVPECL (ECLinPS Plus™ Device) to LVDS is shown below. (Figure 6)

![Figure 6. Capacitive Coupling LVPECL to LVDS](image)
Capacitive Coupling ECL to LVDS Using V\text{OS} Reference Voltage

Some LVDS devices supply offset reference voltage (V\text{OS}), which can be used for capacitive coupling. When the transmission line is very short, a parallel termination should be used and placed as close as possible to the coupling capacitors. (Figure 7)

The Thevenin parallel resistors terminate the transmission line Z near the receiver (Figure 8). Instead of a resistor to V\text{EE}, a resistive path to V\text{CC} and to V\text{EE} (GND) generates the termination of the transmission line. In transmission line theory these resistors are in parallel for high frequency signals. They match the line characteristic impedance (eq. 1).

\[
Z = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2 + R_3}}
\]  
(eq. 1)

The DC condition for point A is V\text{CC} – 2.0 V (eq. 2). The DC levels at the LVDS input (B) are located within the LVDS input common mode range (eq. 3).

\[
A: \frac{R_2 + R_3}{R_1 + R_2 + R_3} = \frac{V_{CC} - 2V}{V_{CC}}
\]  
(eq. 2)

\[
B: \frac{R_3}{R_1 + R_2 + R_3} = \frac{V_{IL}}{V_{CC}}
\]  
(eq. 3)

The amplitude at the LVDS input is decreased dependent on R2 and R3 resistor values.

\[
V_{Input} = \frac{R_3}{R_2 + R_3} \cdot V_{Output}
\]  
(eq. 4)

\[
V_{IH} < 2.0 \text{ V (2.4 V)}
\]  
(eq. 5)

\[
V_{IL} > 0 \text{ V}
\]  
(eq. 6)

Examples:

For 50 \Omega controlled impedance, the resistor values for 2.5 V LVPECL and 3.3 V LVPECL converted to LVDS voltage levels are as follows:

2.5 V LVPECL System

Resistor Values are :

\[
R_1 = 63 \text{ \Omega}
\]
\[
R_2 = 125 \text{ \Omega}
\]
\[
R_3 = 125 \text{ \Omega}
\]

Figure 8. Interfacing LVPECL to LVDS in Thevenin Parallel Termination

Figure 9. +2.5 V LVPECL to LVDS Voltages Levels
3.3 V LVPECL System

Resistor Values are:

\[
\begin{align*}
R1 &= 83 \, \Omega \\
R2 &= 63 \, \Omega \\
R3 &= 63 \, \Omega
\end{align*}
\]

Figure 10. +3.3 V LVPECL to LVDS Voltages Levels

For any other controlled impedance line, the calculation of the resistive divider network is done according to Eq. 1, Eq. 2, and Eq. 3.

Interfacing from LVDS to LVPECL

The input common mode range of the low voltage ECL line receivers are wide enough to process LVDS signals. (Figure 11)

\[
\begin{align*}
Z &= 50 \, \Omega \\
Z &= 50 \, \Omega \\
100 \, \Omega
\end{align*}
\]

Figure 11. Interfacing LVDS to LVPECL

This direct interface is possible for all ECL devices with sufficiently low minimum differential common mode range inputs. A differentially operated receiver’s \( V_{\text{HCMR}} \) minimum must be 1.2 V or less (see device data sheet).

The following devices are LVDS input compatible:

- EP14 LVEL11 LVEL15 SG11
- EP809 LVEL13 LVEL56 SG14
- LVE11 LVEL14 LVEL92 SG16
- LVE14 LVEL16 EL13 SG16VS
- LVP16 LVEL17 EL14 SG53A
- LVEP34 LVEL29 EL17 SG86A
- LVE11 LVEL32 EL29
- LVEP210 LVEL33 EL39
- LVEP210S LVEL37 EL56
- LVE222 LVEL39 EL91
- LVEL05 LVEL40

Interfacing from PECL to LVDS

Interfacing from PECL to LVDS Using Thevenin Parallel Termination

As described for LVPECL, to interface from PECL to LVDS a Thevenin Parallel Termination is used.

Near the receiver, a +5.0 V power supply connection is required. (Figure 12)

\[
\frac{1}{\frac{1}{R1} + \frac{1}{R2+R3}} = Z \quad \text{(eq. 7)}
\]

Figure 12. Interfacing from PECL to LVDS Using Thevenin Equivalent Parallel Termination
The DC termination level at point A is $V_{CC} - 2.0\,\text{V}$. The DC level of input B should be within the LVDS input common mode range.

$$A: \frac{R_2 + R_3}{R_1 + R_2 + R_3} = \frac{V_{CC} - 2\,\text{V}}{V_{CC}} \quad (\text{eq. 8})$$

$$B: \frac{R_3}{R_1 + R_2 + R_3} = \frac{V_{IL}}{V_{CC}} \quad (\text{eq. 9})$$

The LVDS input voltage amplitude ($V_{Input}$) is decreased from $V_{Output}$, which is dependent on $R_2$ and $R_3$ resistor values:

$$V_{Input} = \frac{R_3}{R_2 + R_3} \cdot V_{Output} \quad (\text{eq. 10})$$

$V_{IH} < 2.0\,\text{V} (2.4\,\text{V}) \quad (\text{eq. 11})$

$V_{IL} > 0\,\text{V} \quad (\text{eq. 12})$

Calculations may give non-standard resistor values. When choosing resistors off the shelf, keep in mind to avoid a cutoff condition under worst-case condition.

If a 50 $\Omega$ controlled impedance line is used the following resistor values are useful:

**Examples:**

For 50 $\Omega$ controlled impedance, the resistor values for 5.0 V PECL converted to LVDS voltage levels are as follows:

**5.0 V PECL System**

Resistor Values are:

- $R_1 = 125\,\Omega$
- $R_2 = 42\,\Omega$
- $R_3 = 42\,\Omega$

For any other controlled impedance line the calculation of the resistive divider network is done according to Eq. 7, Eq. 8 and Eq. 9.

**Interfacing from +3.3 V LVDS to +5.0 V PECL**

To translate LVDS signals to PECL a differential ECL device with extended common mode range inputs (e.g., MC100EL17) can be used to process and translate LVDS signals when supplied with 5.0 V $\pm$ 5% supply voltage. (See Figure 14)
Interfacing Between NECL to LVDS

ON Semiconductor has developed level translators to interface between the different voltage levels. The MC100EP90 translates from negative supplied ECL to LVPECL. The interface from LVPECL to LVDS inputs is described above. (Figure 15)

![Figure 15. Interfacing from NECL to LVDS](image1)

To interface from LVDS to negative supplied ECL the common mode range (V_{IHCMR}) of the MC100LVEL91 for −3.3 V supply and the MC100EL91 for −4.5 V/−5.2 V supply is wide enough to process LVDS signals. (See Figure 16)

If $V_{CC} = +5 V \pm 5\%$ supply and a $V_{EE} = −5.2 V \pm 5\%$ supply is available the MC10E1651 can be used.

![Figure 16. Interfacing from LVDS to NECL](image2)

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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada</td>
<td></td>
<td></td>
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<td></td>
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</tbody>
</table>

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